REMARKS

In the Final Office Action of July 25, 2006, the Examiner (1) rejected claims 3, 12, and 19 under § 112, second paragraph; (2) rejected claims 1-3, 5-7, 10-12, 14, and 17-20 as being unpatentable over U.S. Patent No. 6,088,786 ("Feierbach et al.") in view of U.S. Patent No. 6,965,984 ("Seal"), in view of U.S. Patent No. 6,954,873 ("Jain"). In this Response, Applicants cancel claims 3, 12, and 19, amend claims 1, 10, 17 and submit new claims 21-24.

Claims 3, 12, and 19 have been cancelled thereby mooting the § 112, second paragraph, rejections.

Claim 1 has been amended to further require that the "second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor." Thus, per claim 1, the wait signal is actively deasserted by the synchronization unit upon command from the second processor (via the wait release signal). None of the art teaches this limitations. The Examiner conceded that neither Feierbach nor Seal disclose asserting the wait signal to cause the first processor to enter the reduced power or reduced performance mode. Final Office Action page 6. The Examiner, however, turned to Jain as allegedly teaching the claimed wait signal.

Jain teaches the implementation of a wait-state. Figures 2, 3, and 5 in Jain, for example, show the assertion of a wait signal for one clock cycle. Jain explains that such wait states are used to permit a processor to communicate with a slower memory or peripheral device. One of ordinary skill in the art would understand that the wait state signals described in Jain are asserted for a pre-defined period of time and then deasserted. In claim 1, however, the second processor actively causes the first processor to be released from its reduced power or performance mode by asserting a wait release signal to the synchronization unit which then actively causes the wait signal to be de-asserted. One of ordinary skill in the art would understand that Jain's wait signal is deasserted automatically, and not by, as is required by claim 1, a synchronization unit receiving a release signal from another processor thereby causing the synchronization unit to deassert the wait signal. No other art of record satisfies this deficiency of Jain. For

at least this reason, claim 1 and all claims dependent thereon are allowable over the art of record.

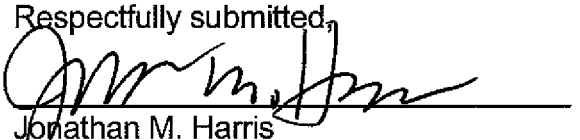
Newly added claim 21 depends from claim 1 and further requires that the "wait signal remains asserted until said synchronization unit deasserts said wait signal." Jain does not teach or even suggest that the wait signal remains asserted until the synchronization unit takes an action which, per claim 1, is based on the second processor asserting a release signal. Instead, the wait signal in Jain is deasserted upon expiration of a predefined number of clock cycles.

Newly added claim 22 recites that the "second processor asserts said wait release signal when said second processor requires support from said first processor." None of the art of record teaches the assertion of such a wait release signal based on a processor requiring support from another processor.

Independent claims 10 and 17 have been amended and are patentable for the same or similar reason as claim 1. Thus, claims 10 and 17 and their respective dependent claims are in condition for allowance for much the same reason as claim 1. Further, claims 23 and 24 have been added to depend from claim 17 and provide additional patentable features.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims), Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,



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